Workflow

● Worked from two ends, then integrated:
  ○ Page-up (lower-level)
  ○ User-down (higher-level)

● Agreed on API to interface between higher level and lower level components, enabling us to work from both ends somewhat independently

● Agreed on using cumulative tail records
Database Design
Pages & Logical Pages

Page ID: index of physical page in bufferpool

Metadata page IDs:

- Indir Page ID
- RID Page ID
- Time Page ID
- Sch. Page ID
- C1 Page ID
- C2 Page ID
- CN Page ID

Data page IDs:

Page: object representing a physical page

Bufferpool:

- Page 1
- Page 2
- Page 3
- Page 4
- ...
- Page M-1
- Page M

Logical page:

- Indir Page ID
- RID Page ID
- Time Page ID
- Sch. Page ID
- C1 Page ID
- C2 Page ID
- ...
Page Ranges

Structure used to manage base and tail pages

Allocated on as-needed basis

page_ranges

Page Range

Base Page

Base Page

Tail Page

Tail Page

Fixed maximum number of base pages (positions reserved on page range creation)

Unlimited tail pages
Table

Connects pages and queries

Manages page ranges and allocates pages as needed

Site of physical page storage

**Index**: maps column values to RIDs O(1) access time

**Page Directory** (hash table): maps RID to physical location O(1) access time
Index

Hash tables for each data column index: O(1) access

Vital for query performance: Selecting 10,000 records went from finishing on the order of minutes (using scanning) to on the order of seconds

indices[i]: maps a value to an array of RIDs of the records with that value in the i’th column
Query Logic: Select & Sum

Select and Sum (Read Focused)

Insert (Write Focused)
Query Logic: Updates & Deletes
Performance
Hardware

- **(Windows)**
  - Intel Core i7, 1.8GHz, 8GB, 8MB L3 Cache

- **(Mac)**
  - Apple M1, 3.2 GHz, 16GB, 12 MB L2 Cache

Workloads:
- **custom**
Hardware

- (Windows)
  Intel Core i7, 1.8GHz, 8GB, 8MB L3 Cache

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Workloads: custom
Testing: Page Range Size

Workload: __main__.py
Hardware: Dual-Core Intel Core i7, 2.5GHz, 16GB, 4 MB L3 Cache
Q & A